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6-29-01  
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Docket No.: 202009US-2 DIV

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF

Shigenobu MAEDA : EXAMINER:

SERIAL NO: NEW APPLICATION

FILED: HEREWITH : GROUP ART UNIT:

FOR: MANUFACTURING METHOD OF  
SEMICONDUCTOR WAFER,  
SEMICONDUCTOR MANUFACTURING  
APPARATUS, AND SEMICONDUCTOR  
DEVICE

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS  
WASHINGTON, D.C. 20231

SIR:

Prior to examination on the merits, please amend the above-identified patent application as follows:

IN THE CLAIMS

Please cancel without prejudice or disclaimer Claims 1-20.

Please add Claims 21-24 as follows:

*Sub B* 21. A method of manufacturing a semiconductor device for building a circuit composed of combined plural circuit elements into a semiconductor chip, comprising:

*A /* expressing a layout pattern of said circuit by using mask patterns respectively prepared for said plural circuit elements.

*B* 22. The method of manufacturing a semiconductor device according to Claim 21, wherein